- Timing From Microseconds to Hours
- Astable or Monostable Operation
- Adjustable Duty Cycle
- TTL-Compatible Output Can Sink or Source Up To 200 mA

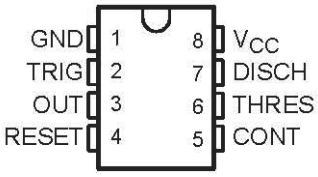
Description/ordering information

These devices are precision timing circuits capable of producing accurate time delays or oscillation. In the time-delay or monostable mode of operation, the timed interval is controlled by a single external resistor and capacitor network. In the astable mode of operation, the frequency and duty cycle can be controlled independently with two external resistors and a single external capacitor.

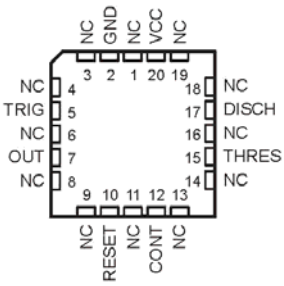
The threshold and trigger levels normally are two-thirds and one-third, respectively, of Vcc. These levels can be altered by use of the control-voltage terminal. When the trigger input falls below the trigger level, the flip-flop is set and the output goes high. If the trigger input is above the trigger level and the threshold input is above the trigger level and the threshold input is above the threshold level, the flip-flop is reset and the output is low. The reset (RESET) input can override all other inputs and can be used to initiate a new timing cycle. When RESET goes low, the flip-flop is reset and the output goes low. When the output is low, a low-impedance path is provided between discharge (DISCH) and ground.

The output circuit is capable of sinking or sourcing current up to 200 mA. Operation is specified for supplies of 5V to 15V. With a 5-V supply, output levels are compatible with TTL inputs.

NE555…D, P, PS, OR PW PACKAGE
SA555… D OR P PACKAGE
SE555… D, JG, OR P PACKAGE
(TOP VIEW)



SE555…FK PACKAGE
(TOP VIEW)



NC-NO internal Connection

Description/ordering information (continued)

ORDERING INFORMATION

TA	VTHRES MAX VCC=15V	PACKAGE †		ORDERABLE PARTNUMBER	TOP-SIDE MARKING
0°C to 70°C	11.2V	PDIP(P)	Tube of 50	NE555P	NE555P
		SOIC (D)	Tube of 75	NE555D	NE555
			Reel of 2500	NE555DR	
		SOP(PS)	Reel of 2000	NE555PSR	N555
		TSSOP(PW)	Tube of 150	NE555PW	N555
			Reel of 2000	NE555PWR	
-40°C to 85°C	11.2V	PDIP (P)	Tube of 50	SA555P	SA555P
		SOIC (D)	Tube of 75	SA555D	SA555
			Reel of 2000	SA555DR	
-55°C to 125°C	10.6V	PDIP (P)	Tube of 50	SE555P	SE555P
		SOIC (D)	Tube of 75	SE555D	SE555D
			Reel of 2500	SE555DR	
		CDIP (JG)	Tube of 50	SE555JG	SE555JG
		LCCC (FK)	Tube of 55	SE555FK	SE555FK

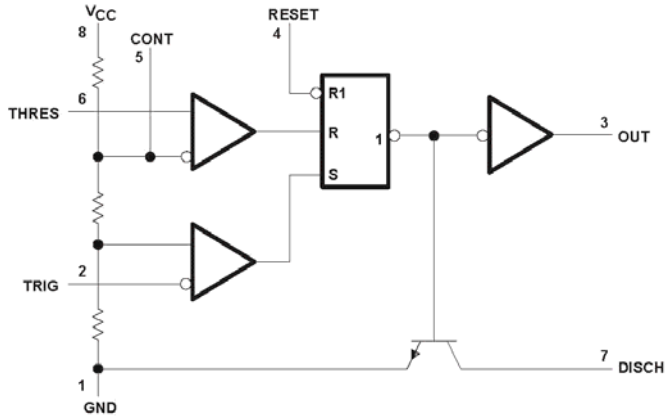
†Package drawing, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.artschip.com.

FUNCTION TABLE

RESET	TRIGGER VOLTAGE‡	THRESHOLD VOLTAGE‡	OUTPUT	DISCHARGE SWITCH
Low	Irrelevant	Irrelevant	Low	On
High	<1/3 V_{DD}	Irrelevant	High	Off
High	>1/3 V_{DD}	>2/3 V_{DD}	Low	On
High	>1/3 V_{DD}	<2/3 V_{DD}	As previously established	

‡ Voltage levels shown are nominal.

Function block diagram



Pin numbers shown are for the D,JG,P,PS,and PW packages.
NOTE A: RESET can override TRIG, which can override THRES.

Absolute maximum ratings over operating free-air temperature range (unless otherwise note) †

Supply voltage, Vcc (see Note 1)……18V
Input voltage (CONT, RESET, THRES, and TRING)……Vcc
Output Current…… ±225mA
Package thermal impedance, Θ_{JA} (see Notes 2 and 3): D package……97°C/W
P package……85°C/W
PS package……95°C/W
PW package……149°C/W
Package thermal impedance, Θ_{JC} (see Notes 4 and 5): FK package……5.61°C/W
JG package……14.5°C/W
Operating virtual junction temperature, TJ……150°C
Case temperature for 60 seconds: FK package……260°C
Lead temperature 1,6mm (1/16inch) from case for 60 seconds: JG package……300°C
Storage temperature range, Tstg……-65°C to 150°C

†Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Notes: 1. All voltage values are with respect to GND.

2. Maximum power dissipation is a function of $T_{J(max)}$. Θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D=(T_{J(max)}-T_A)/\Theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.
4. Maximum power dissipation is a function of TJ(max), Θ_{JC}, and TC. The maximum allowable power dissipation at any allowable case temperature is $P_D=(TJ(max)-Tc)/\Theta_{JA}$. Operating at the absolute maximum TJ of 150°C can affect reliability.
5. The package thermal impedance is calculated in accordance with MIL-STD-883.

Recommended operating conditions

			MIN	MAX	UNIT
Vcc	Supply voltage	SA555,NE555	4.5	16	V
		SE555	4.5	18	
V_I	Input voltage (CONT, RESET, THRES, and TRIG)			V_{CC}	V
I_O	Output Current			±200	mA
T_A	Operating free-air temperature	NE555	0	70	℃
		SA555	-40	85	
		SE555	-55	125	

Electrical characteristics, Vcc = 5V to 15V, T_A=25℃ (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SE555			NE555 SA555			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
THRES voltage level	Vcc=15V		9.4	10	10.6	8.8	10	11.2	V
	Vcc=5V		2.7	3.3	4	2.4	3.3	4.2	
THRES current (see Note 6)				30	250		30	250	nA
TRIG voltage level	Vcc=15V		4.8	5	5.2	4.5	5	5.6	V
		T_A=-55℃ to 125℃	3		6				
	Vcc=5V		1.45	1.67	1.9	1.1	1.67	2.2	
		T_A=-55℃ to 125℃			1.9				
TRIG current	TRIG at 0V			0.5	0.9		0.5	2	μA
RESET voltage level			0.3	0.7	1	0.3	0.7	1	V
	T_A=-55℃ to 125℃				1.1				
RESET current	RESET at Vcc			0.1	0.4		0.1	0.4	mA
	RESET at 0V			-0.4	-1		-0.4	-1.5	
DISCH switch off-state current				20	100		20	100	nA
CONT voltage (open circuit)	Vcc=15V		9.6	10	10.4	9	10	11	V
		TA=-55℃ to 125℃	9.6		10.4				
	Vcc=5V		2.9	3.3	3.8				
		TA=-55℃ to 125℃	2.9		3.8	2.6	3.3	4	
Low-level output voltage	Vcc=15V, I_{OL}=10mA			0.1	0.15		0.1	0.15	V
		TA=-55℃ to 125℃			0.2				
	Vcc=15V, I_{OL}=50mA			0.4	0.5		0.4	0.75	
		TA=-55℃ to 125℃			1				
	Vcc=15V, I_{OL}=100mA			2	2.2		2	2.5	
		TA=-55℃ to 125℃			2.7				
	Vcc=15V, I_{OL}=200mA			2.5			2.5		
	Vcc=5V, I_{OL}=3.5mA	TA=-55℃ to 125℃			0.35				
	Vcc=5V, I_{OL}=5mA			0.1	0.2		0.1	0.35	
		TA=-55℃ to 125℃			0.8				
	Vcc=5V, IOL=8mA			0.15	0.25		0.15	0.4	
High-level output voltage	Vcc=15V I_{OH}=-100mA		13	13.3		12.75	13.3		V
		TA=-55℃ to 125℃	12						
	Vcc=15V I_{OH}=-100mA			12.5			12.5		
	Vcc=15V I_{OH}=-100mA		3	3.3		2.75	3.3		
		TA=-55℃ to 125℃	2						
Supply Current	Output low, No load	Vcc=15V		10	12		10	15	mA
		Vcc=5V		3	5		3	6	
	Output high No load	Vcc=15V		9	10		9	13	
		Vcc=5V		2	4		2	5	

NOTE 6: This parameter influences the maximum value of the timing resistors R_A and R_B in the circuit of Figure 12. For example, when Vcc=5V, the maximum Value is R=R_A+R_B ≈3.4MΩ, and for Vcc=15V, the maximum value is 10MΩ。

Operating characteristics, Vcc=5V and 15V

Parameter		Test Conditions †	SE555			NE555 SA555			Unit
			MIN	TYP	MAX	MIN	TYP	MAX	
Initial error of timing interval‡	Each timer, monostable§	T_A=25°C		0.5	1.5*		1	3	%
	Each timer, astable¶			1.5			2.25		
Temperature coefficient of timing interval	Each timer, monostable§	T_A=Min to Max		30	100*		50		ppm/°C
	Each timer, astable¶			90			150		
Supply-voltage sensitivity of timing interval	Each timer, monostable§	T_A=25°C		0.05	0.2*		0.1	0.5	%/V
	Each timer, astable¶			0.15			0.3		
Output-pulse rise time		C_L=15pF T_A=25°C		100	200*		100	300	Ns
Output-pulse fall time		C_L=15pF T_A=25°C		100	200*		100	300	ns

*On products compliant to MIL-PRF-38535, this parameter is not production tested.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

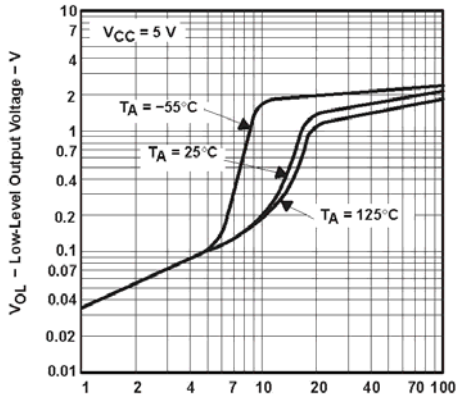
‡ Timing interval error is defined as the difference between the measured value and the average value of a random sample from each process run.

§ Values specified are for a device in a monostable circuit similar to Figure 9, with the following component values: R_A=2kΩ to 100kΩ C=0.1μF.

¶ Values specified are for a device in an astable circuit similar to Figure 12. With the following component values: R_A=1kΩ to 100KΩ, C=0.1μF.

TYPICAL CHARACTERISTICS †

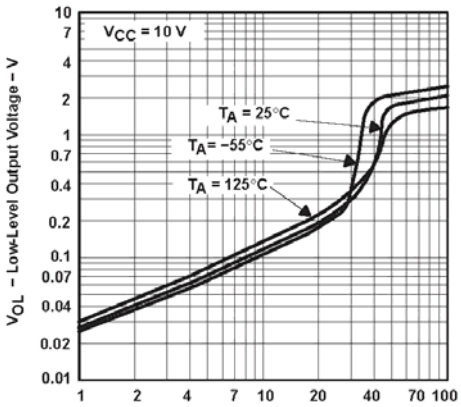
LOW-LEVEL OUTPUT VOLTAGE
VS
LOW-LEVEL OUTPUT CURRENT



I_{OL}-Low-Level Output Current-mA

Figure 1

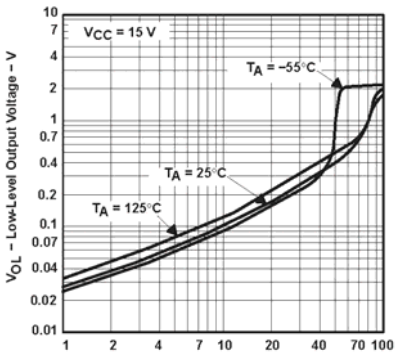
LOW-LEVEL OUTPUT VOLTAGE
VS
LOW-LEVEL OUTPUT CURRENT



I_{OL}-Low-Level Output Current – mA

Figure 2

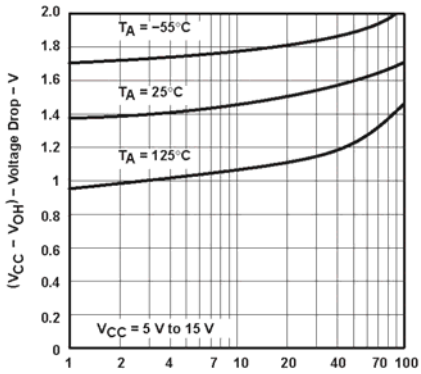
LOW-LEVEL OUTPUT VOLTAGE
VS
LOW-LEVEL OUTPUT CURRENT



IOL-Low-Level Output Current – mA

Figure 3

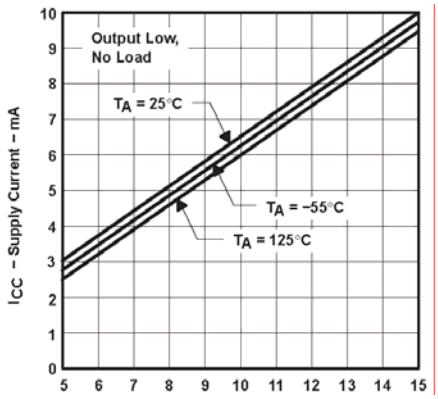
DROP BETWEEN SUPPLY VOLTAGE AND OUTPUT
VS
HIGH-LEVEL OUTPUT CURRENT



IOH – High-Level Output Current –mA

Figure 4

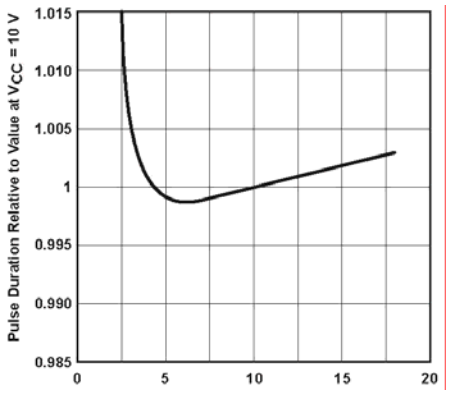
SUPPLY CURRENT
VS
SUPPLY VOLTAGE



Vcc-Supply Voltage-V

Figure 5

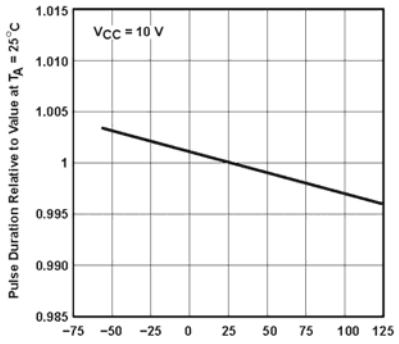
NORMALIZED OUTPUT PULSE DURATION
(MONOSTABLE OPERATION)
VS
SUPPLY VOLTAGE



Vcc-Supply Voltage –V

Figure 6

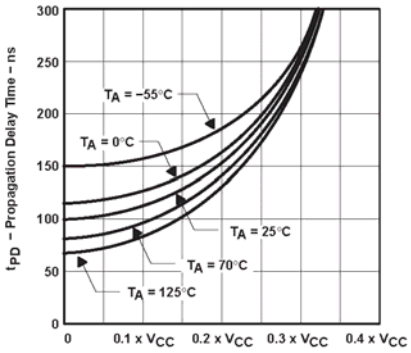
NORMALIZED OUTPUT PULSE DURATION
(MONOSTABLE OPERATION)
VS
FREE-AIR TEMPERATURE



TA-Free-Air Temperature -°C

Figure 7

PROPAGATION DELAY TIME
VS
LOWEST VOLTAGE LEVEL
OF TRIGGER PULSE



Lowest Voltage Level of Trigger Pulse

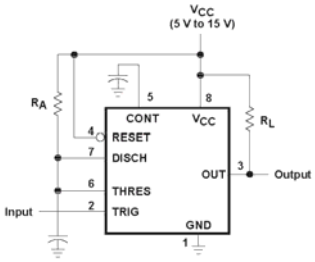
Figure 8

| Data for temperatures below 0°C and above 70°C are applicable for SE555 series circuits only.

APPLICATION INFORMATION

Monostable operation

For monostable operation, any of these timers can be connected as shown in Figure 9. if the output is low, application of a negative-going pulse to the trigger (TRIG) sets the flip-flop ($\overline{Q}$ goes low), drivers the output high, and turns off Q1, Capacitor C then is charged through RA until the voltage across the capacitor reaches the threshold voltage of the threshold (THRES) input. If TRIG has returned to a high level, the output of the threshold comparator resets the flip-flop ($\overline{Q}$ goes high), drives the output low, and discharges C through Q1.

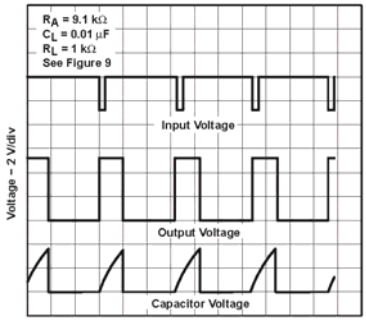


Pin numbers shown are for the D,JG,P,PS, and PW packages.

Figure 9. Circuit for Monostable Operation

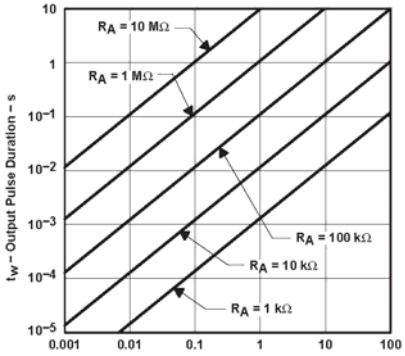
Monostable operation is initiated when TRIG voltage falls below the trigger threshold. Once initiated, the sequence ends only if TRIG is high at the end of the timing interval. Because of the threshold level and saturation voltage of Q1, the output pulse duration is approximately t_W=1.1RAC. Figure 11 is a plot of the time constant for various values of RA and C. The threshold levels and charge rates both are directly proportional to the supply voltage, Vcc. The timing interval is , therefore, independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to RESET and reinitiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when RESET is low. To prevent false triggering, when RESET is not used, it should be connected to Vcc.



Time-0.1 ms/div

Figure 10. Typical Monostable Waveforms



C-Capacitance-µF

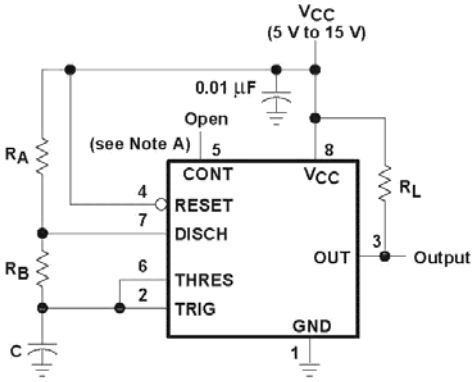
Figure 11. Output Pulse Duration vs Capacitance

APPLICATION INFORMATION

Astable operation

As shown in Figure 12, adding a second resistor, R_B, to the circuit of Figure 9 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multivibrator. The capacitor C charges through R_A and R_B and then discharges through R_B only. Therefore, the duty cycle is controlled by the values of R_A and R_B.

This astable connection results in capacitor C charging and discharging between the threshold-Voltage level (≈0.67 x Vcc) and the trigger-voltage level (≈0.33 x Vcc). As in the monostable circuit, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage.



Pin numbers shown are for the D, JG, P, PS, and PW packages.

Note A: Decoupling CONT voltage to ground with a capacitor can improve operation. This should be evaluated for individual applications.

Figure 12. Circuit for Astable Operation

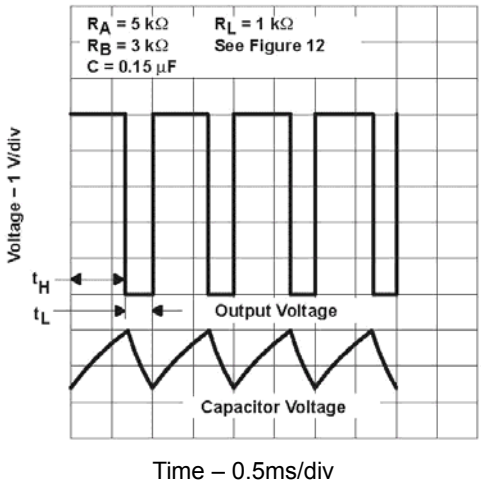


Figure 13. Typical Astable Waveforms

Astable Operation (Continued)

Figure 13 shows typical waveforms generated during astable operation. The output high-level duration t_H and low-level duration t_L can be calculated as follows:

$$t_H = 0.693\ (R_A + R_B)C$$

$$t_L = 0.693\ (R_B)C$$

Other useful relationships are shown below.

$$\text{Period} = t_H + t_L = 0.693\ (R_A + 2R_B)\ C$$

$$\text{Frequency} \approx 1.44 / (R_A + 2R_B)\ C$$

Output driver duty cycle $= t_L / (t_H + t_L) = R_B / (R_A + 2R_B)$

Output waveform duty cycle

$= t_H / (t_H + t_L) = 1 - R_B / (R_A + 2R_B)$

Low – to – high ratio $= t_L / t_H = R_B / (R_A + R_B)$

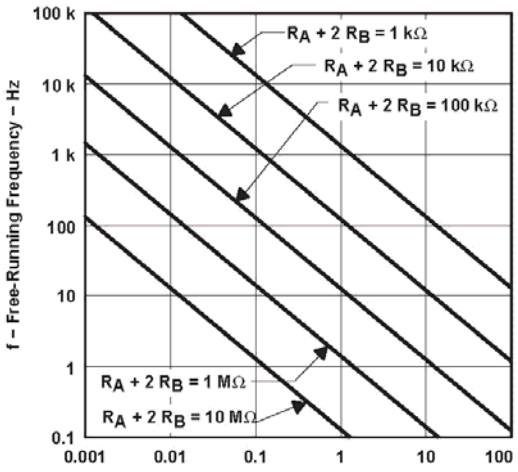
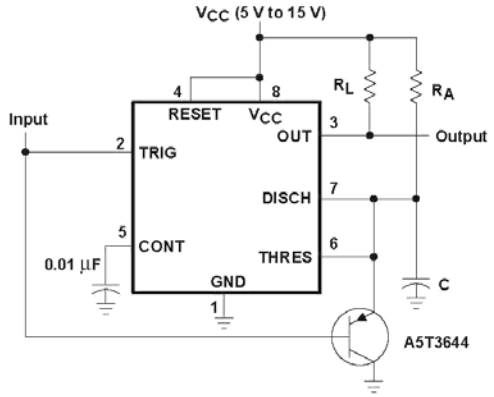


Figure 14. Free-Running Frequency

APPLICATION INFORMATION

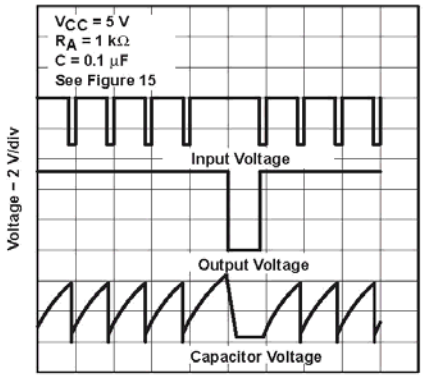
Missing-pulse detector

The circuit shown in Figure 15 can be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is retriggered continuously by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse as shown in Figure 16.



Pin numbers shown are shown for the D, JG, P, PS, and PW package.

Figure 15. Circuit for Missing-Pulse Detector

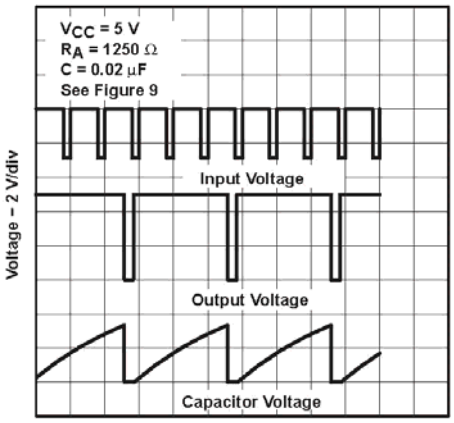


Time – 0.1ms/div

Figure 16. Completed-Timing Waveforms For Missing-Pulse Detector

Frequency divider

By adjusting the length of the timing cycle, the basic circuit of Figure 9 can be made to operate as a frequency divider. Figure 17 shows a divide-by-three circuit that makes use of the fact that retriggering cannot occur during the timing cycle.



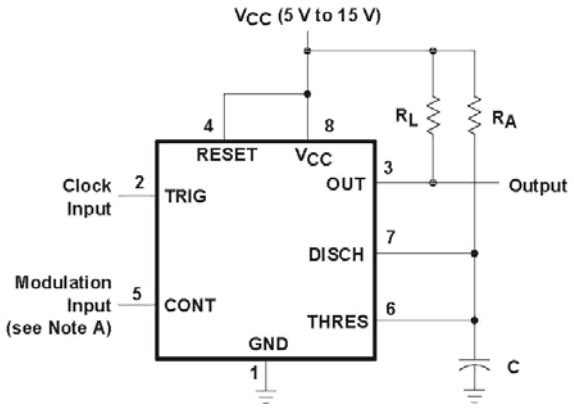
Time – 0.1 ms/div

Figure 17. Divide-by-Three Circuit Waveforms

Pulse-width modulation

The operation of the timer can be modified by modulating the internal threshold and trigger voltages, which is accomplished by applying and external voltage (or current) to CONT. Figure 18 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. Figure 19 shows the resulting output pulse-width modulation. While a sine-wave modulation signal is shown, any wave shape could be used.

APPLICATION INFORMATION



Pin numbers shown are for the D, JG, P, PS, and PW packages.

Note A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 18. Circuit for Pulse-Width Modulation

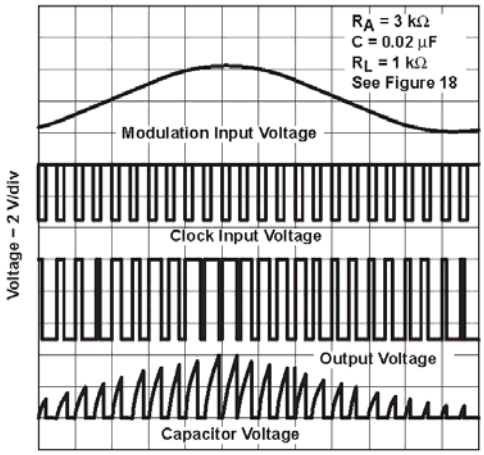
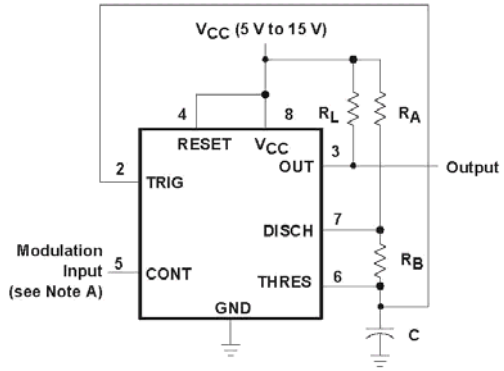


Figure 19. Pulse-Width-Modulation Waveforms

Pulse-position modulation

As shown in Figure 20, any of these timers can be used as a pulse-position modulator. This application modulates the threshold voltage and, thereby, the time delay, of a free-running oscillator. Figure 21 shows a triangular-wave modulation signal for such a circuit; however, any wave shape could be used.



Pin numbers shown are for the D, JG, P, PS, and PW packages.

NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

Figure 20. Circuit for Pulse-Position Modulation

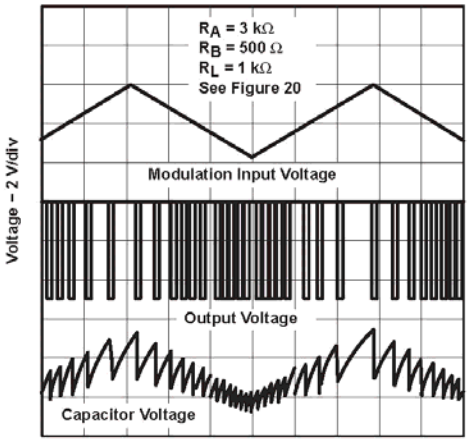
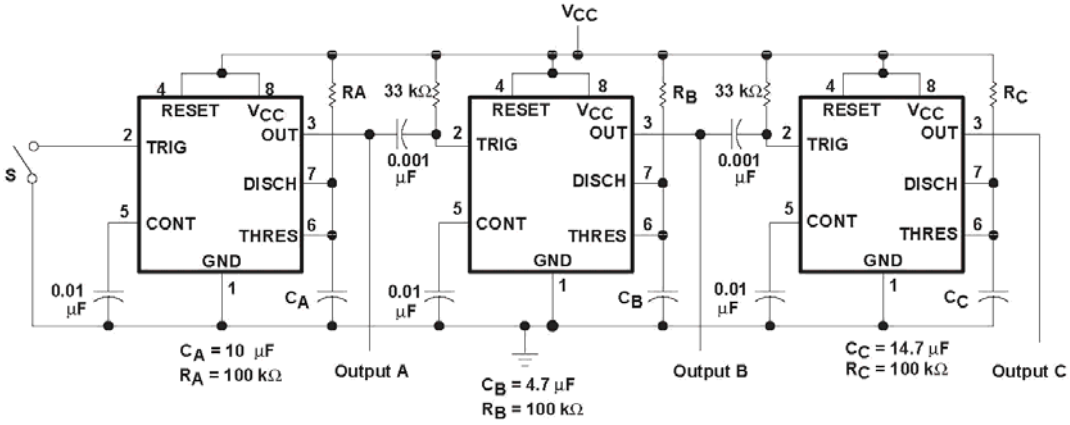


Figure 21. Pulse – Position – Modulation Waveforms

APPLICATION INFORMATION

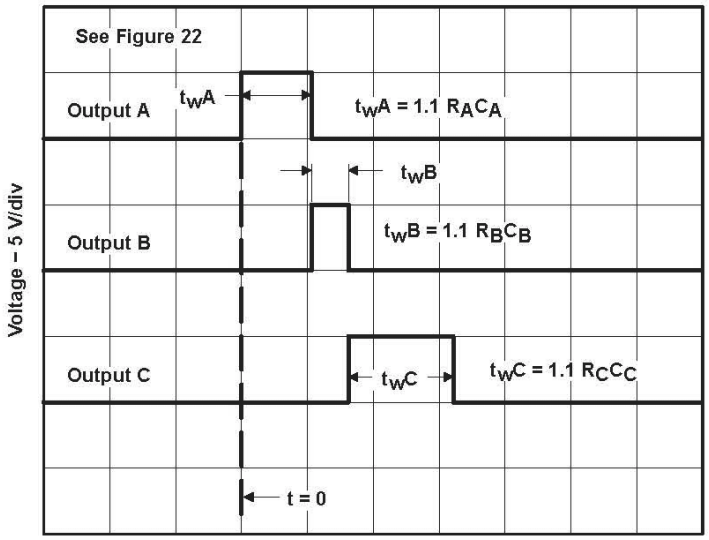
Sequential timer

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications, such as test equipment, require activation of test signals in sequence. These timing circuits can be connected to provide such sequential control. The timers can be used in various combinations of astable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. Figure 22 shows a sequencer circuit with possible applications in many systems, and Figure 23 shows the output waveforms.



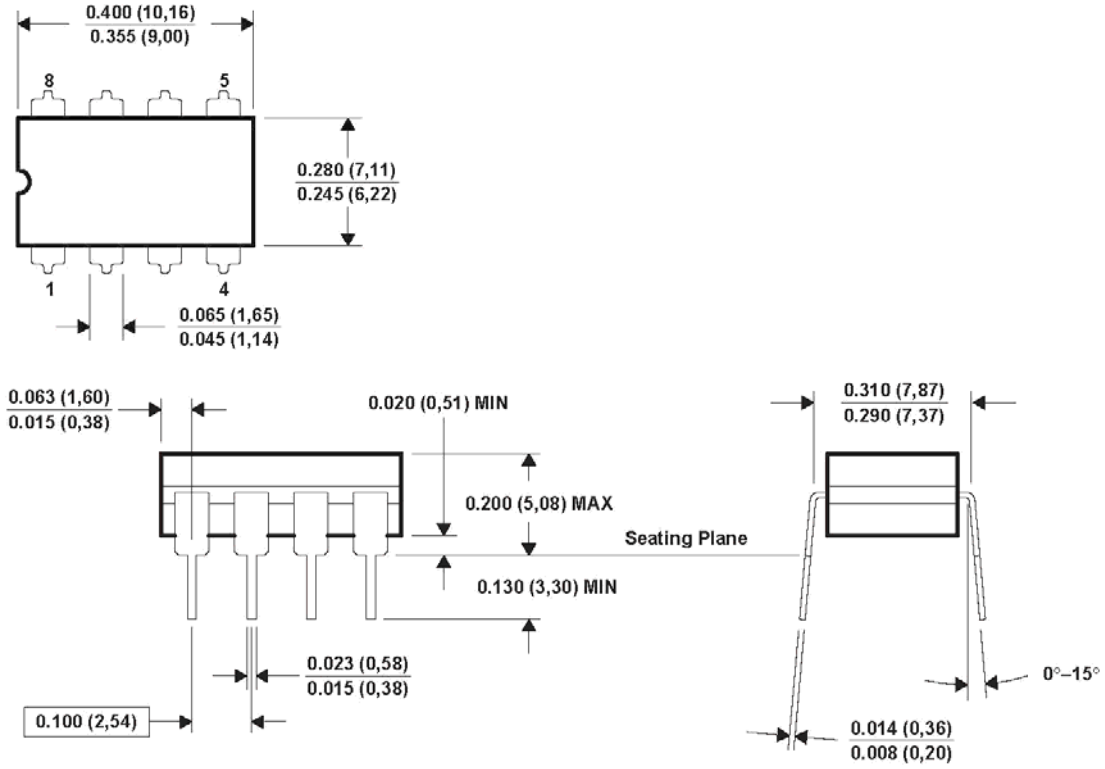
Pin numbers shown are for the D, JG, P, PS, and PW packages.
NOTE A: S closes momentarily at t =0.

Figure 22. Sequential Timer Circuit



t – Timer – 1 s/div

Figure 23. Sequential Timer Waveforms

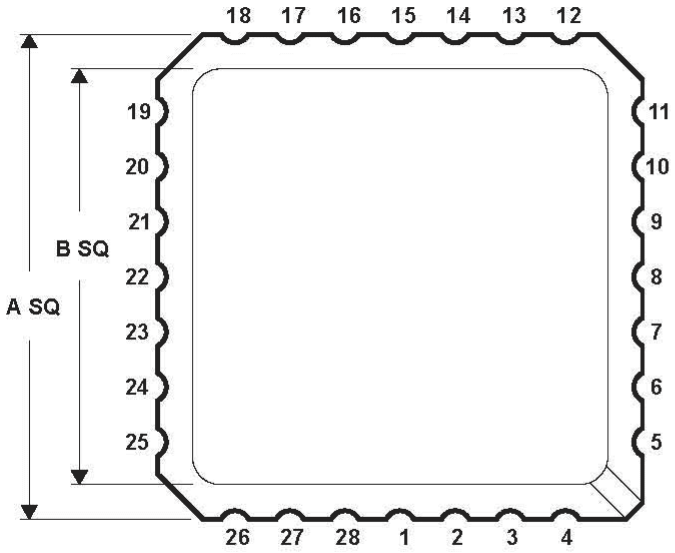


4040107/C 08/96

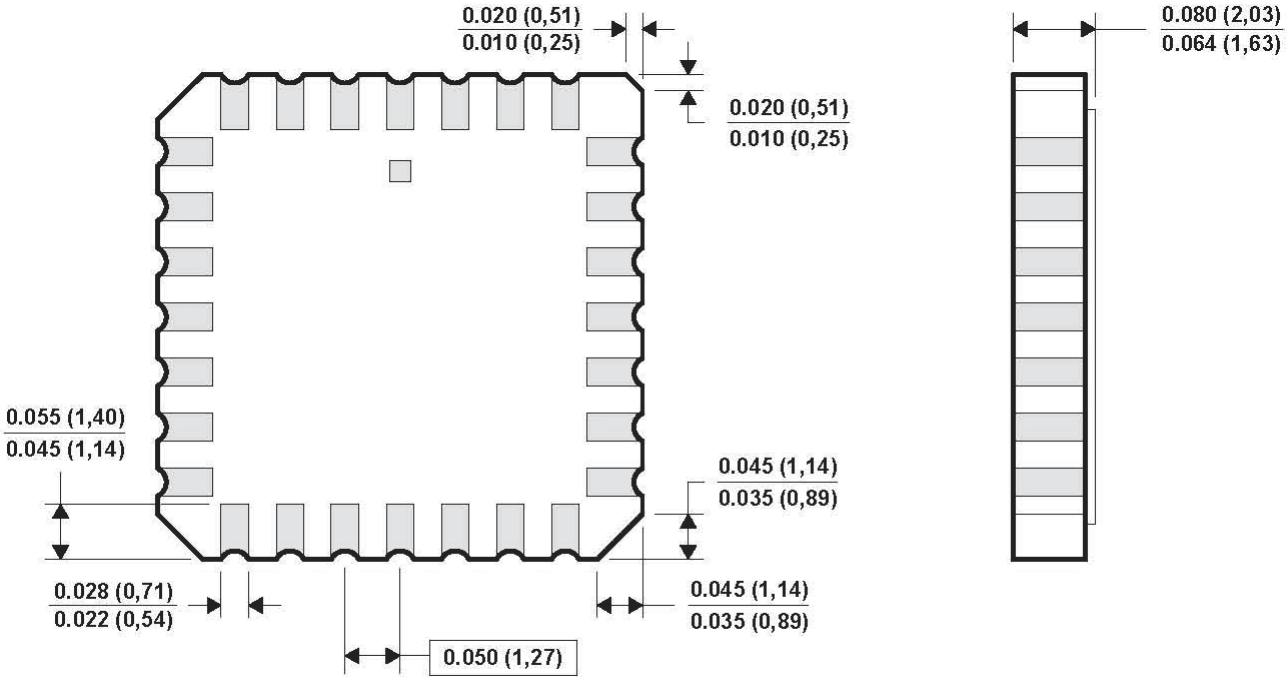
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

FK(S-CQCC-N)** **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).

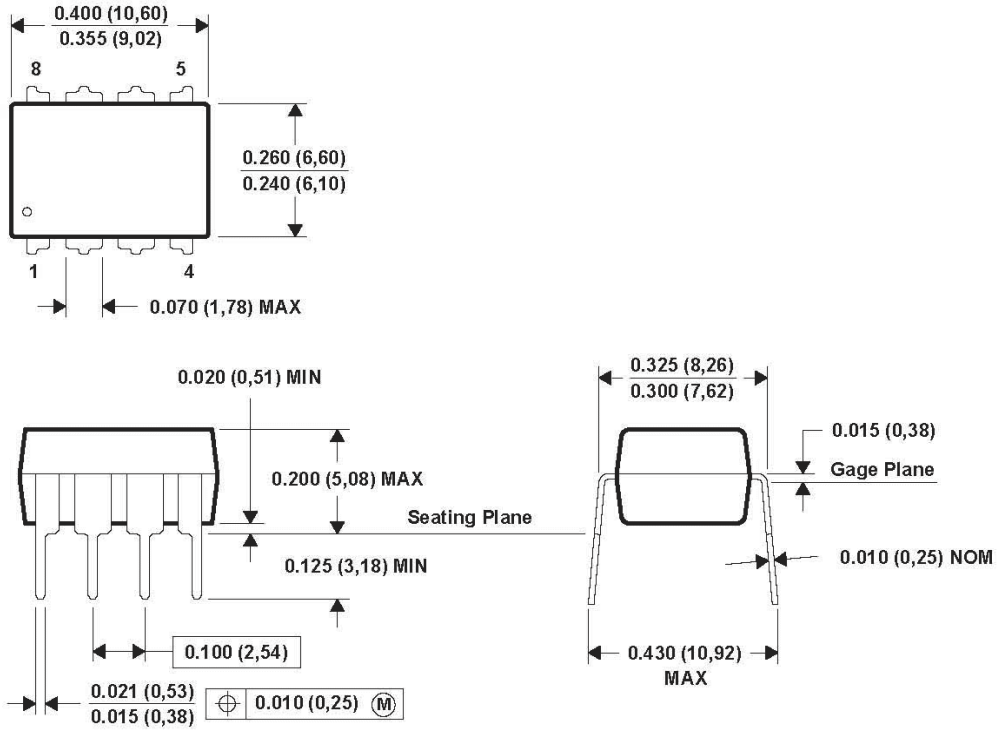
B. This drawing is subject to change without notice.

C. This package can be hermetically sealed with a metal lid.

D. The terminals are gold plated.

E. Falls within JEDEC MS-004.

P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



4040082/D 05/98

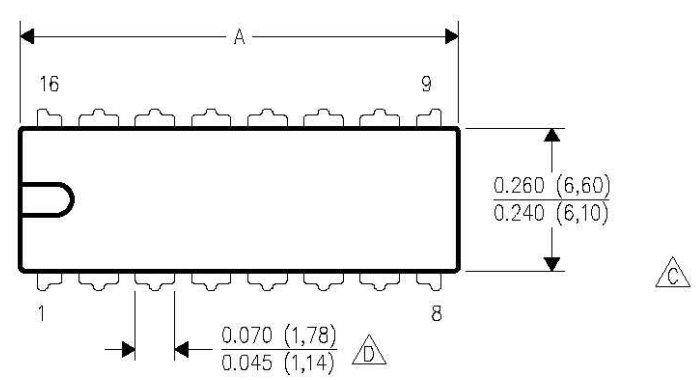
NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

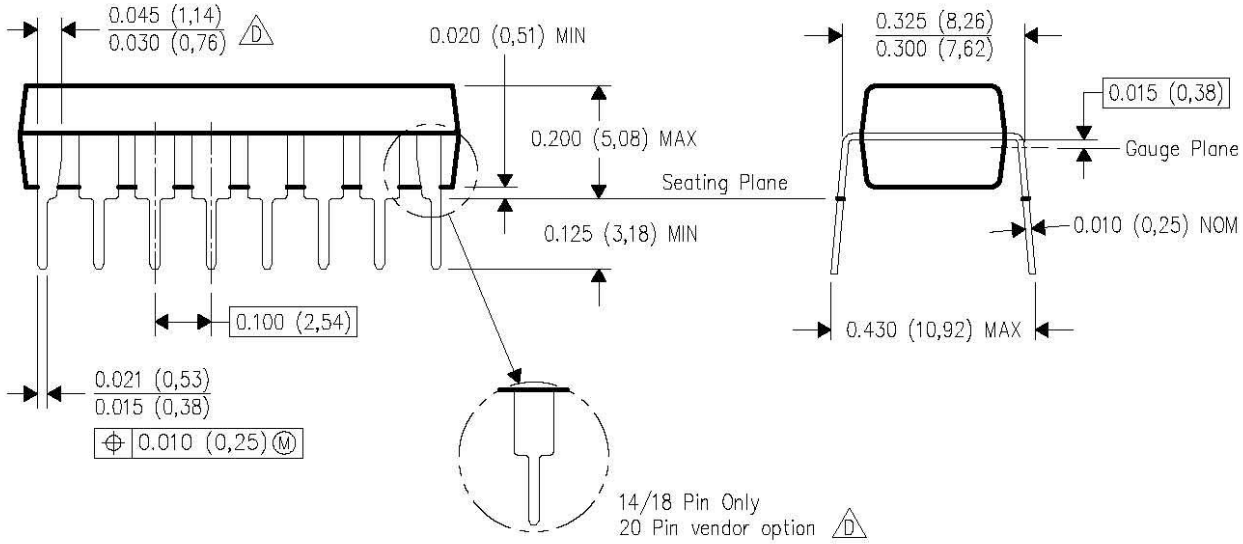
C. Falls within JEDEC MS-001

N (R-PDIP-T **) **PLASTIC DUAL-IN-LINE PACKAGE**

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).

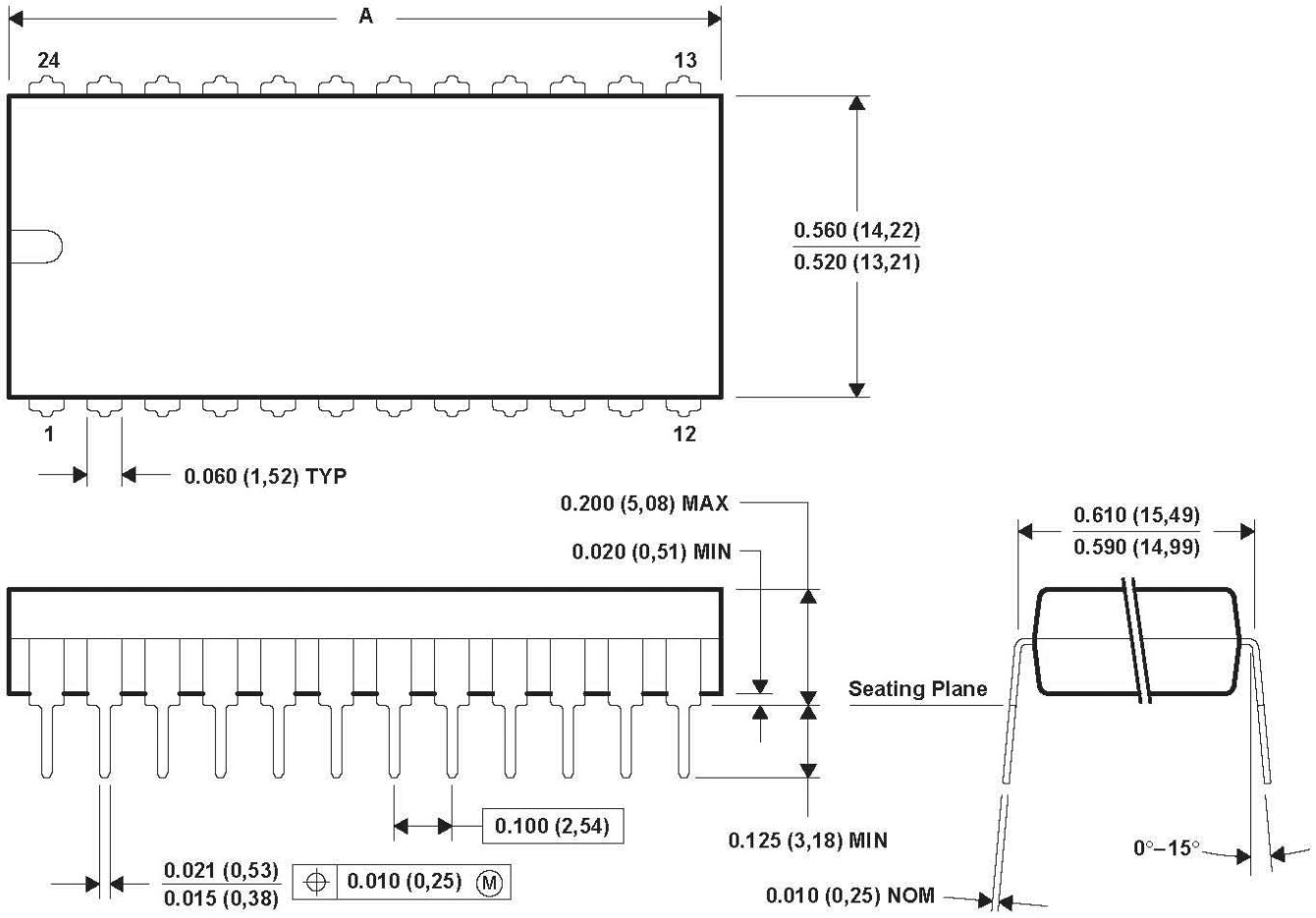
B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).

D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

N (R-PDIP-T **) **PLASTIC DUAL-IN-LINE PACKAGE**

24 PIN SHOWN



DIM \ PINS **	24	28	32	40	48	52
A MAX	1.270 (32,26)	1.450 (36,83)	1.650 (41,91)	2.090 (53,09)	2.450 (62,23)	2.650 (67,31)
A MIN	1.230 (31,24)	1.410 (35,81)	1.610 (40,89)	2.040 (51,82)	2.390 (60,71)	2.590 (65,79)

4040053 / B 04/95

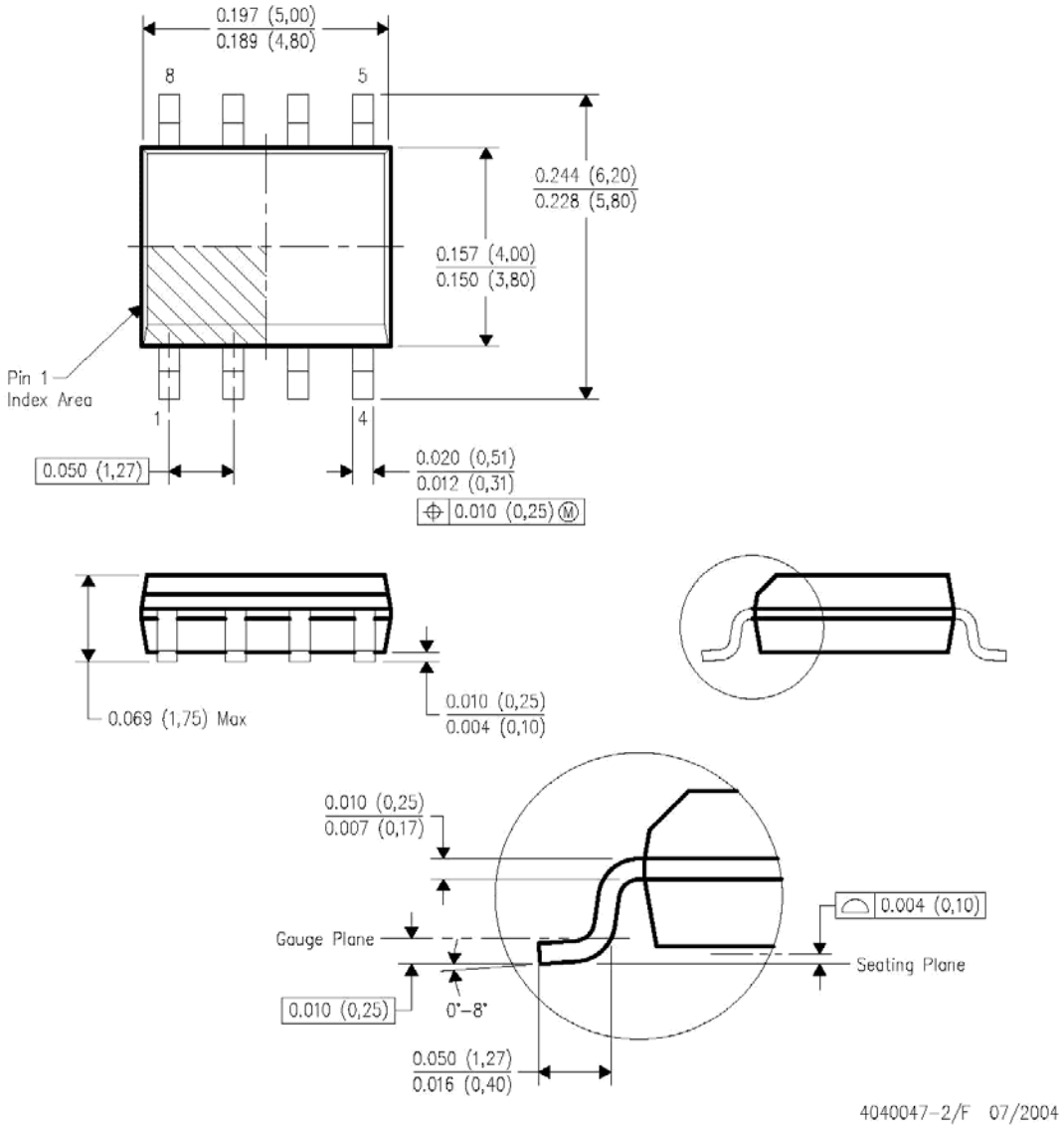
NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Falls within JEDEC MS-011

D. Falls within JEDEC MS-015 (32 pin only)

D (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).

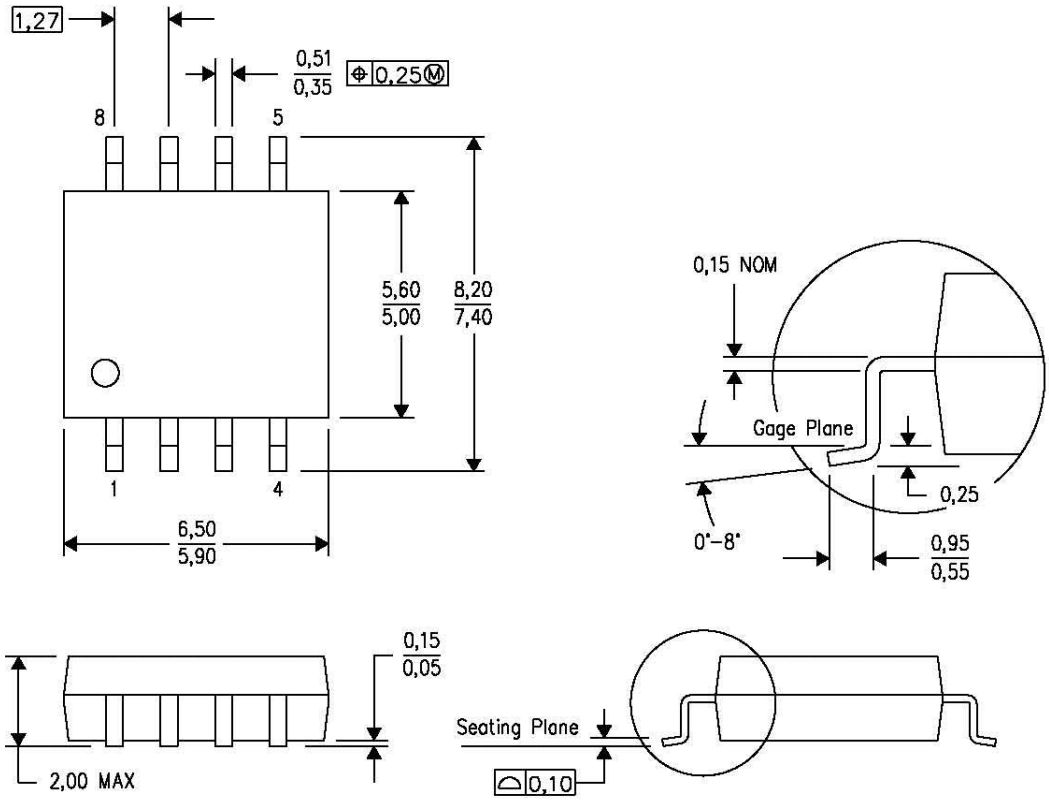
B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).

D. Falls within JEDEC MS-012 variation AA.

MECHANICAL DATA

PS (R-PDSD-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

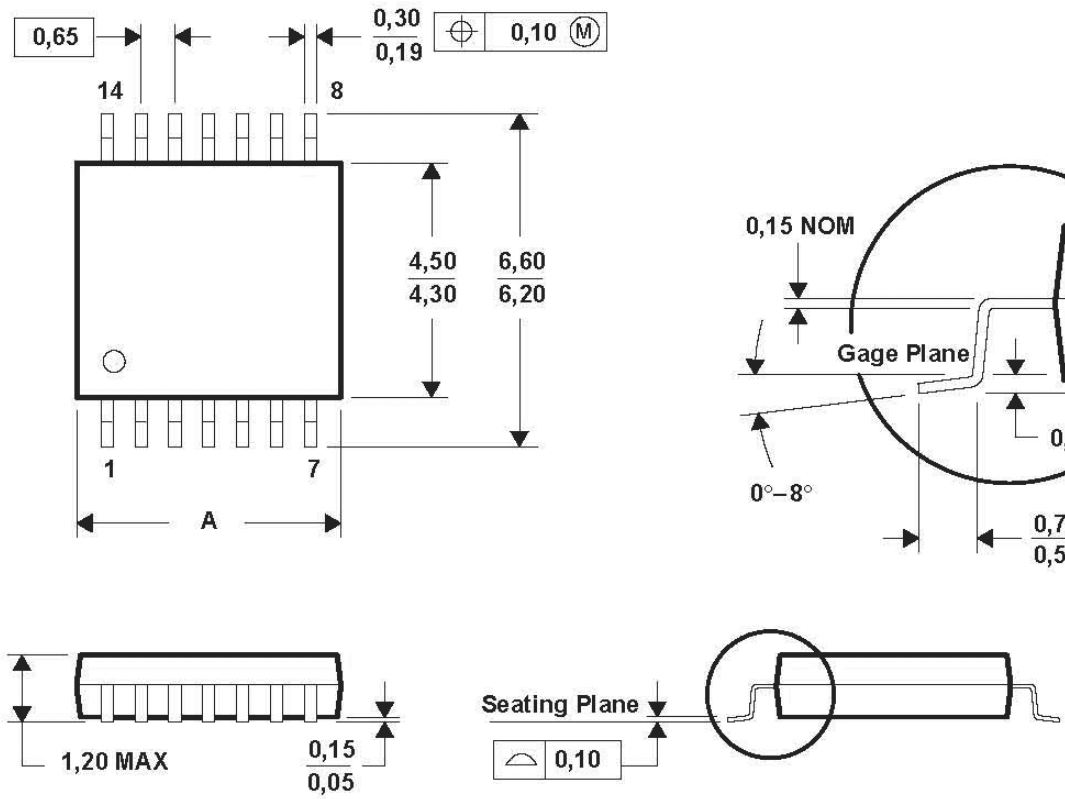
NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion, not to exceed 0.15.

PW (R-PDSO-G **) **PLASTIC SMALL-OUTPUT PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Body dimensions do not include mold flash or protrusion not to exceed 0.15.

D. Falls within JEDEC MO-153